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Abstract

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A 145MHz Low Phase-Noise Capacitive Silicon Micromechanical Oscillator

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Abstract

This paper reports on the implementation and characterization of a low phase-noise oscillator based on a very high quality factor (Q) 145MHz capacitive silicon micromechanical resonator. The utilized resonator is a silicon bulk acoustic resonator (SiBAR) operating in its first width-extensional mode with a maximum $Q_{unloaded}$~74,000 that is specifically optimized for low motional impedance. The sustaining circuitry is a 3.6mW CMOS transimpedance amplifier (TIA) that uses common source topology with local shunt-shunt feedback. The measured phase-noise of the oscillator at *1kHz* offset from the carrier is *-111dBc/Hz* with phase-noise floor reaching below *-133dBc/Hz.*

Introduction

High Q silicon micromechanical oscillators are viable timing solutions for modern communication systems as they offer superior close-to-carrier phase-noise in a small form factor, and potential for integration with integrated circuits [1,2]. High frequency oscillators (>100MHz) reduce the up-conversion ratio in frequency synthesizer, thus, paving the way for higher performance and lower power transceivers. Additionally, high Q resonators will enable higher resolution in ADCs by offering low-jitter integrated timing source.

The main obstacle complicating the realization of high frequency silicon micromechanical timing oscillators is the loss of the capacitive resonator; the *motional resistance* of the silicon resonator increases rapidly as the frequency scales to the upper VHF range. This large resistance makes the realization of low-power high-frequency silicon micromechanical oscillators very challenging. The motional impedance can be minimized by increasing the transduction area or reducing the capacitive gap, both of which have practical limitations [3]. Simulation of the frequency response of a SiBAR in ANSYS reveals that there is an optimum thickness for which the motional impedance can be minimized.

In this work, a 145MHz low phase-noise oscillator based on a very high-Q SiBAR that is specially optimized for low motional impedance is presented. The resonator is first modeled in ANSYS and its frequency response is simulated using a model that emulates the electrostatic transduction mechanism in the capacitive gaps. The result is used to find the appropriate resonator thickness t for which the motional impedance is near minimum. The resonator is fabricated on a low-resistivity SOI substrate with $t=15\mu m$ device layer thickness using the high aspect-ratio poly and single-crystalline silicon process (HARPSS). The measured motional impedance and Q of the 27µm wide and 270µm long SiBAR at polarization voltage of V_p=14V are 2.4kΩ and 51,000, respectively. The resonator is then wirebonded to a 3.6mW two-stage TIA that is designed in 0.18µm 1P6M CMOS process.

Oscillator Block Diagram

The block diagram of the micromechanical oscillator is shown in Fig. 1. The frequency of oscillation is determined by the 145MHz SiBAR with a polarization voltage of 14V.

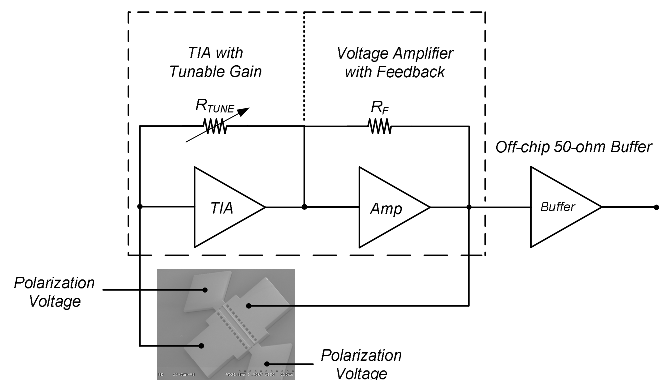

Figure 1: The block diagram of the 145MHz micromechanical oscillator

The sustaining amplifier consists of two parts: TIA and a voltage amplifier. The TIA is a simple common source stage with tunable shunt-shunt feedback. The voltage amplifier is another common source stage with local shunt-shunt feedback to provide additional gain and 180º phase-shift.

Silicon Resonator Design, Optimization and Fabrication

A. SiBAR Design and Optimization

The utilized resonator is a SiBAR device that operates in its fundamental width-extensional mode. A SiBAR is comprised of a high aspect-ratio single-crystal-silicon bar resonator and two trench-refilled polysilicon electrodes on either side of the bar that are separated by very narrow vertical gaps from the bar (Fig. 2.a). A DC polarization voltage, V_p, is applied to the resonator to reduce the motional impedance and prevent frequency doubling. The resonant frequency is determined by the width of the bar (Fig. 2.b and c).

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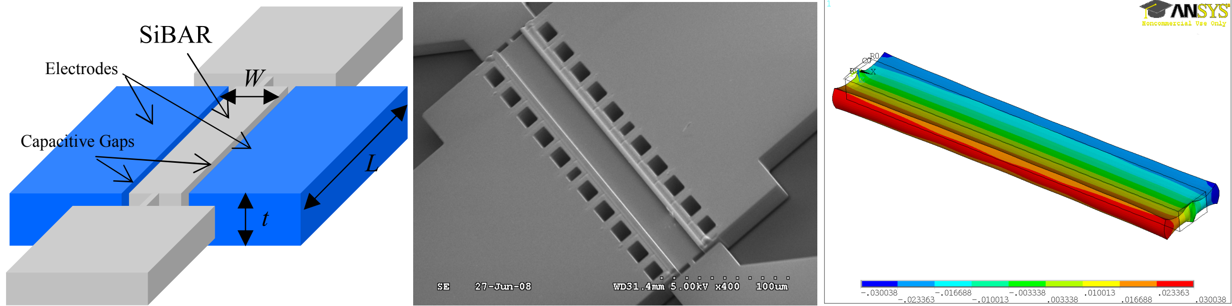

Figure 2: (a) Structure, (b) SEM view, and (c) simulated width-extensional mode shape of the 145MHz SiBAR device in ANSYS ($t=15\mu m$).

The motional impedance is proportional to the fourth power of the gap, and inversely proportional to the square of V_p, and transduction area A [4]:

$$R_m \propto \frac{g^4}{Q.V_p^2.A} \qquad (1)$$

Lowering the motional impedance of a device with given dimensions requires that either the gap size is reduced or V_p is increased. Both of these methods are unattractive due to the fabrication issues and inherent incompatibility of most IC technologies with high voltages. Therefore, increasing the transduction area (mainly through increasing the thickness of the resonator or by arraying resonators) or using a material with high dielectric constant in the gap [5] appears to be the path toward lower motional impedance resonators. The latter, however, may negatively affect Q and significantly increases the static capacitance of the resonator; thereby, making it unsuitable for low-power low phase-noise oscillators.

While increasing the thickness initially lowers motional impedance of the resonator, as the thickness-to-width ratio increases, wavy patterns start appearing in the resonant mode shape of the device which lowers the transduction efficiency. Further increase in the device thickness causes the motional impedance to start rising again [3].

The value of the silicon thickness that minimizes the insertion loss (while keeping the thickness less than 30µm for ease of manufacturing) was determined from ANSYS simulations of a model of the complete device, including electromechanical transduction in the capacitive gaps. Different types of element models available in ANSYS were used for the various components of the resonator. An orthotropic model, SOLID45, was used for the silicon bar, while electromechanical transduction in each of the resonator's capacitive gaps was modeled by an array of TRANS126 elements, generated automatically by the EMTGEN macro. TRANS126 is an element that implements electromechanical transduction using a simple capacitive model. A number of resistors and capacitors were also added to model the test setup used for resonator testing (Fig. 3). This model makes it possible to simulate the frequency response of a SiBAR of arbitrary dimensions.

Each simulation consists of a static analysis, which is needed to account for the effect of the DC polarization voltage, followed by a harmonic analysis over a specified frequency range. This particular set of analyses, combined with the inclusion of the electrostatic gap in model, provides more comprehensive and more accurate information about the behavior of the complete device than is obtainable from a simple modal analysis. In particular, the simulation results include the values of all the node voltages, which makes it possible to generate plots of the voltage gain $A_v = v_{out}/v_{in}$ over the specified range of frequencies. Several parameters indicative of the resonator performance can then be obtained from those plots, including the magnitude of the resonant peak, which is related to the insertion loss of the device.

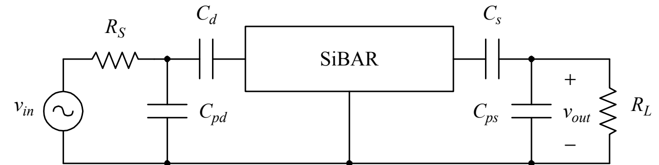

Figure 3: Circuit equivalent of the ANSYS model. C_s and C_d model the gap capacitances, C_{ps} and C_{pd} the parasitic pad capacitances, R_S.and R_L the equivalent internal resistances of the measurement equipment.

Simulations of a set of SiBARs of fixed length (270 µm) and width (27 µm) were used to generate the plot in Fig. 4, which shows the values of $|A_v|$ at resonance as a function of device thickness. The optimal range of thickness values that minimizes the insertion loss in the device is clearly identifiable in the plot (15-20µm).

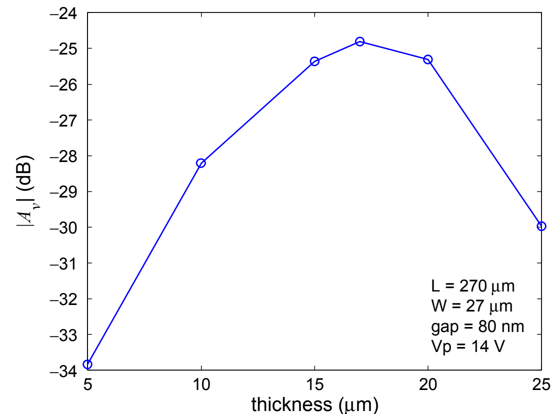

Figure 4: Value of $|A_v|$ at resonance vs. device thickness.

B. Fabrication Procedure

The SiBAR device was fabricated using the HARPSS process flow [3] on a p-type SOI wafer with a device layer thickness as predicted by ANSYS and a low resistivity of 0.005 Ω.cm. The resonator lateral dimensions were defined using deep reactive ion etching. A transduction gap of ~80 nm was realized on this device (Fig. 5). The input and output electrodes, made of polysilicon, were doped heavily with boron. The wafer-level packaging of this device can be done using the thin-film packaging process flow outlined in [6].

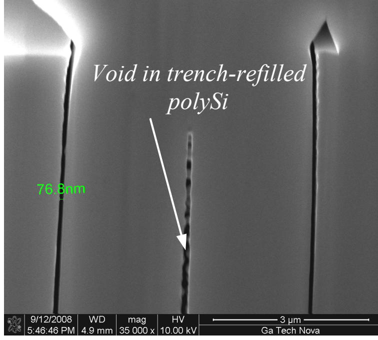

Figure 5: SEM cross section of the SiBAR showing a gap of ~77nm.

Sustaining Amplifier Design

The sustaining amplifier is a two-stage CMOS TIA (Fig. 6). Due to the large motional impedance and input/output parasitic capacitance of the resonator, unlike the TIAs used for low loss high frequency piezoelectric resonators, the TIA gain and 3dB bandwidth has to increase simultaneously. To increase the gain of the TIA beyond the required 80dBΩ without significant increase in power consumption, the signal is passed through additional voltage amplifier with fixed gain. Local shunt-shunt feedback is also used in this stage to improve the 3dB-bandwidth and linearity of the amplifier. The result is a two-stage amplifier in which the first stage uses common-source topology with tunable shunt-shunt feedback and acts as the TIA. The second stage provides additional voltage gain and 180º phase-shift. The gain tuning is realized through an externally-controlled NMOS resistor.

Measurement

The measured frequency response of the fabricated SiBAR shows maximum Q ~ 74,000 at 145MHz with V_p=2V (Fig. 7). The resulting $f.Q$ product, ~1.1×10^{13}, is comparable to that of quartz resonators (~1.6×10^{13}). After increasing V_p to 14V the motional impedance is reduced to 2.4kΩ (Fig. 8), which makes the device suitable for low-power oscillators. The drop in Q at higher V_p is attributed to a series parasitic resistance, R_{load}, in the equivalent electrical model (Fig. 6):

$$\frac{Q_{res}}{Q_{measured}} \propto \frac{R_m + R_{load} + R_s}{R_m} \qquad (2)$$

where Q_{res} is the intrinsic mechanical Q of the resonator, R_s is the resistance of silicon bar, R_{load} is the parasitic series resistance that loads the Q, and R_m is the motional resistance of the resonator that becomes smaller with larger V_p. For this resonator, R_{load} is extracted to be ~1.07kΩ.

The measured temperature behavior of the SiBAR is shown in Fig. 9. The temperature coefficient of frequency (TCF) is −19.2 ppm/C. This smaller TCF value compared to our previous work [3, 6] can be explained by the higher doping concentration of the silicon device layer used in this work [7].

The sustaining circuitry is fabricated in a 0.18µm 1P6M CMOS process and measures 600µm×300µm, of which only 70µm×40µm is occupied by the sustaining amplifier (Fig. 10). An off-chip 50Ω buffer is used to interface with the measurement equipments. The TIA provides more than 80dBΩ at 150MHz with 1.5pF input/output capacitance while consuming 2mA from 1.8V supply. The resonator and IC are interfaced through wirebond.

The oscillator phase-noise is measured in vacuum using an Agilent E5500 phase-noise analyzer system. The measured phase-noise is *-111dBc/Hz* at *1kHz* offset from the carrier and extends below *-133dBc/Hz* at far-from-carrier (Fig. 11). The oscillation power is -9dBm. This is within the resonator linear operating range. Close-to-carrier phase-noise performance of this oscillator meets the GSM phase-noise specification.

The oscillator performance is summarized in Table I and compared with the performance of other capacitive micromechanical oscillators.

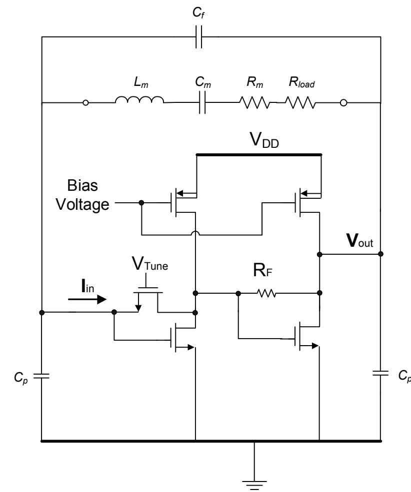

Figure 6: Overall schematic of the TIA interfaced with the SiBAR.

Conclusions

A 145MHz capacitive silicon micromechanical oscillator based on a high-Q SiBAR device is presented, which to the authors' knowledge is the highest frequency micromechanical oscillator reported to-date using a capacitive resonator. The resonator design and thickness are optimized for low motional impedance and high Q. This optimization enables low power operation at high frequency. The sustaining

circuitry consists of a 3.6mW two-stage TIA in 0.18µm CMOS with local shunt-shunt feedback in each stage. Close-to-carrier phase-noise performance is measured *-111dBc/Hz* that meets the GSM standard phase-noise specification.

Acknowledgment

The authors would like to thank Mr. Q. Qin and Dr. S. Pourkamali for valuable discussions about SiBAR devices.

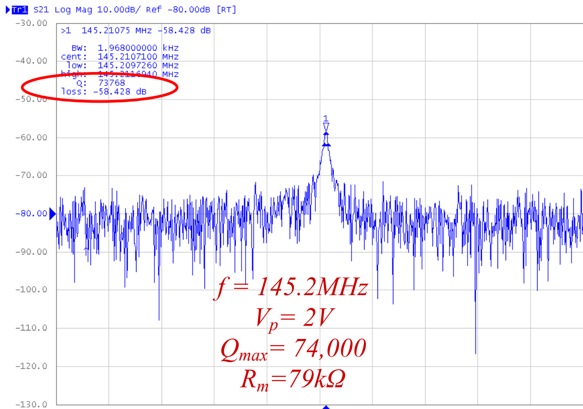

Figure 7: Measured frequency response of the 145MHz SiBAR (highest *Q*).

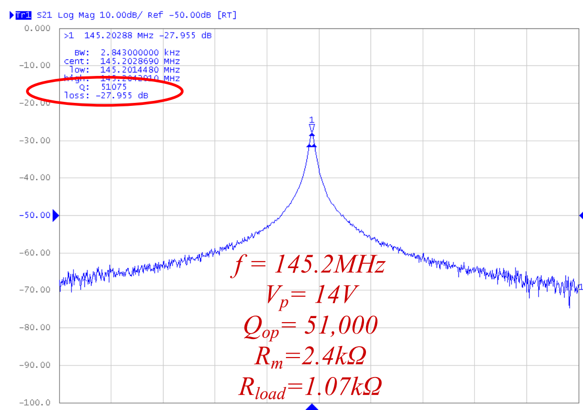

Figure 8: Measured frequency response of the 145MHz SiBAR at V_p=14V.

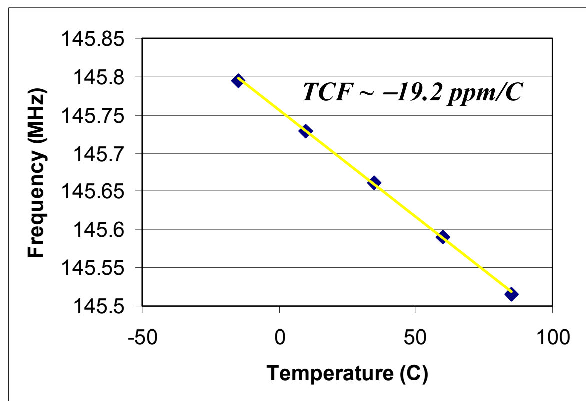

Figure 9: Measured temperature behavior of the 145MHz SiBAR.

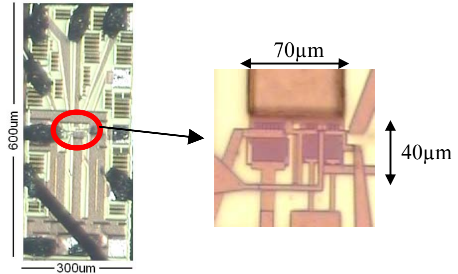

Figure 10: Micrograph of CMOS die. Magnified view shows the active area.

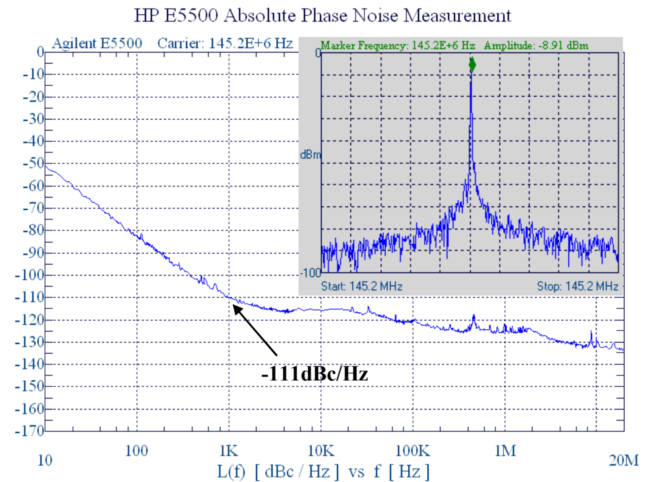

Figure 11: Measured spectrum and phase-noise of the 145MHz oscillator.

Table I: Comparison of capacitive micromechanical oscillators

Oscillator	[4] 61MHz	[2] 103MHz	This Work Scaled to 61MHz	This Work Scaled to 103MHz	This Work 145MHz
PN @ 1kHz (dBc/Hz)	-110	-108	-119	-114	-111
PN floor (dBc/Hz)	-132	-136	-141	-136	-133
f_0 (MHz)	61	103	145		
Resonator Q_{op}	48,000	80,000	51,000		
V_p (V)	12	18	14		
IC Process	0.35µm	0.18µm	0.18µm		

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